ABSTRACT

Output data of a device under test (DUT) is obtained at timing of both rising and falling edges of a clock output from the DUT, and output data of a DDR type device is fetched in synchronization with the clock. A semiconductor test apparatus comprises a clock side time interpolator 20 which obtains clocks input from a DUT 1 by a plurality of strobes of constant timing intervals and which outputs the clocks as time-sequential level data, a data side time interpolator 20 which obtains output data input from the DUT 1 by a plurality of strobes of constant timing intervals and which outputs the output data as time-sequential level data, and an edge selector 30 which switches the time-sequential level data obtained by the time interpolators 20 and selectively outputs level data indicating rising and/or falling edges of the level data.